HARDWARE

REFERENCE DESIGN

WWW.UNICORE.COM

UM680 Series

GNSS High-Precision RTK Positioning Module

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Revision History

Version	Revision History	Date
R1.0	First release.	May 2025

Document Status

Releases	Status Descriptions	Current Status
Primary	This is a pre-release version with target specifications that are subject to revision.	
Alpha release	This is an alpha release version, which has been preliminarily tested and verified. The content may undergo minor modifications based on user feedback and further testing.	
Production release	The document contains the complete and final specifications.	√

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Foreword

This document provides the hardware reference design of Unicore UM680 series modules.

The UM680 series modules consist of the following models:

Product	Main model	Sub-Model
UM680 series	UM680A (automotive)	UM680A-12
		UM680A-13
	UM680 (industrial)	UM680-12

Target Readers

This document applies to technicians who are familiar with GNSS receivers.

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1 Block Diagram

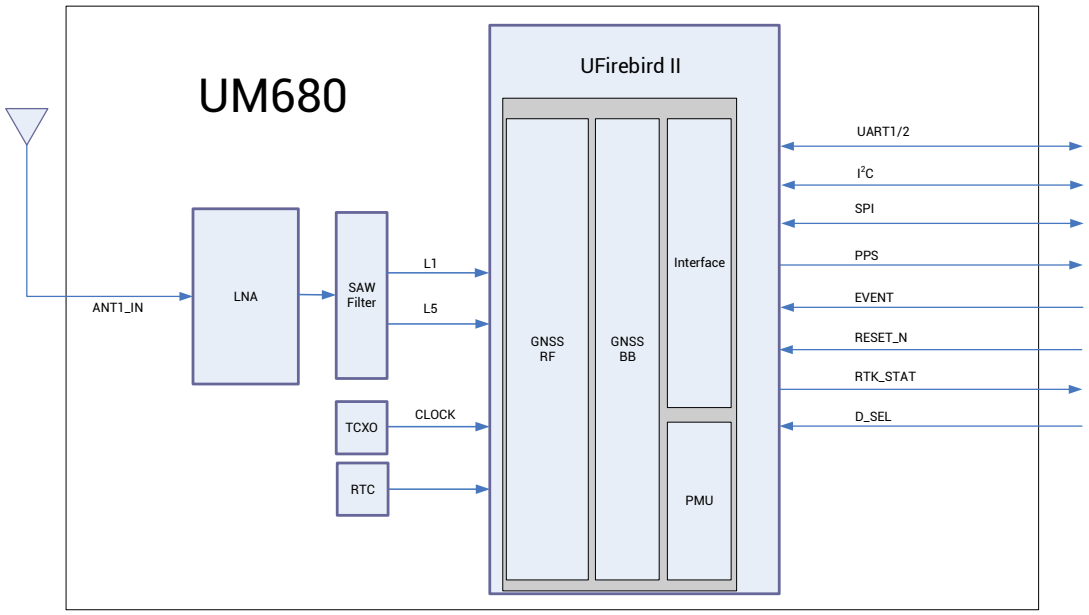


Figure 1-1 UM680 Block Diagram[1]

[1] I²C and SPI are reserved interfaces.

2 UM680 Peripheral Design

- Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.
- Connect all the GND pins to the ground.
- Leave the IO pins open if not used.
- Recommended to add TVS anti-surge protection at the power input. Add ESD protection at the used pins.

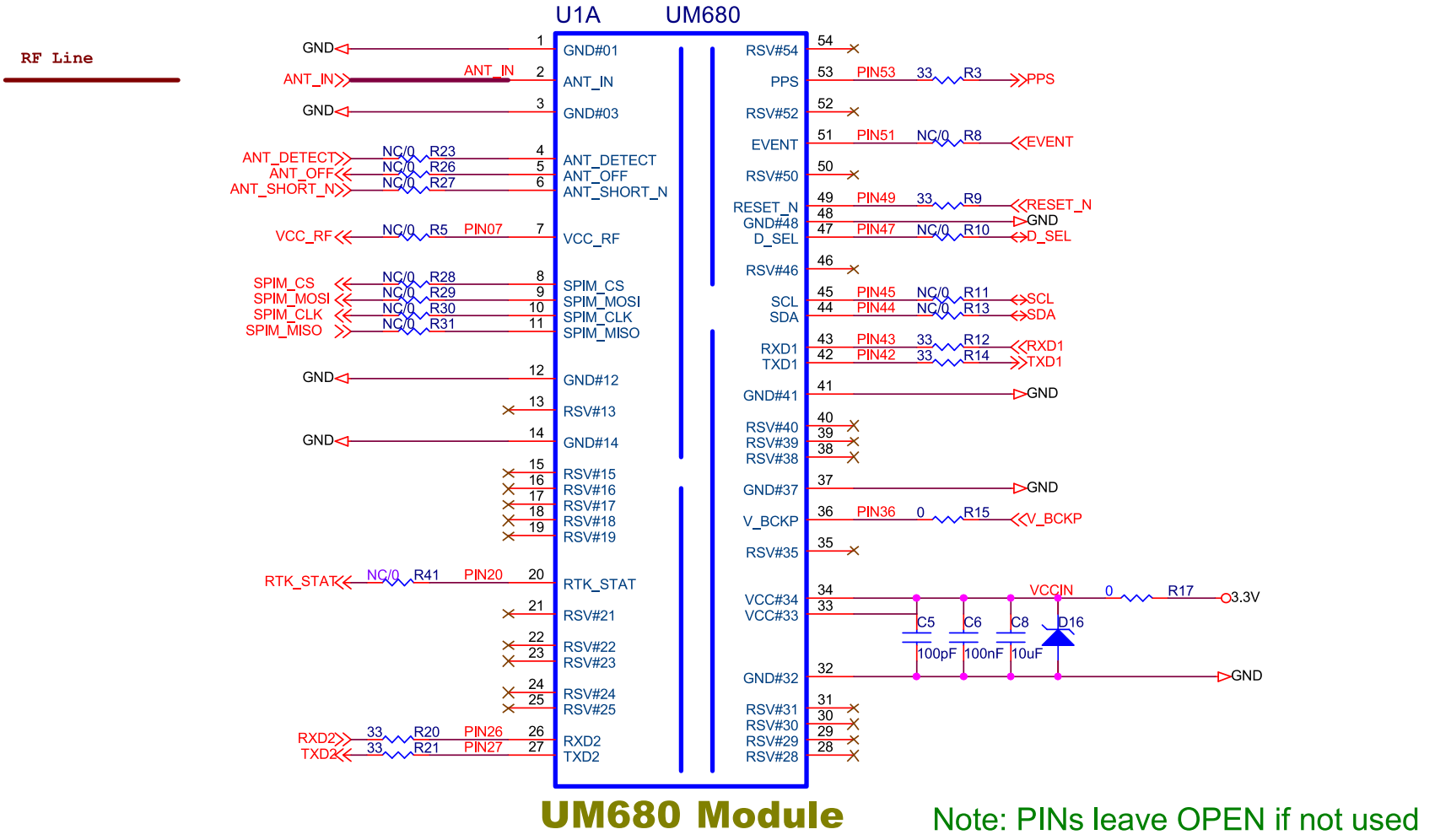


Figure 2-1 UM680 Peripheral Design

The GND pads at the bottom of the module should be grounded to ensure heat dissipation.

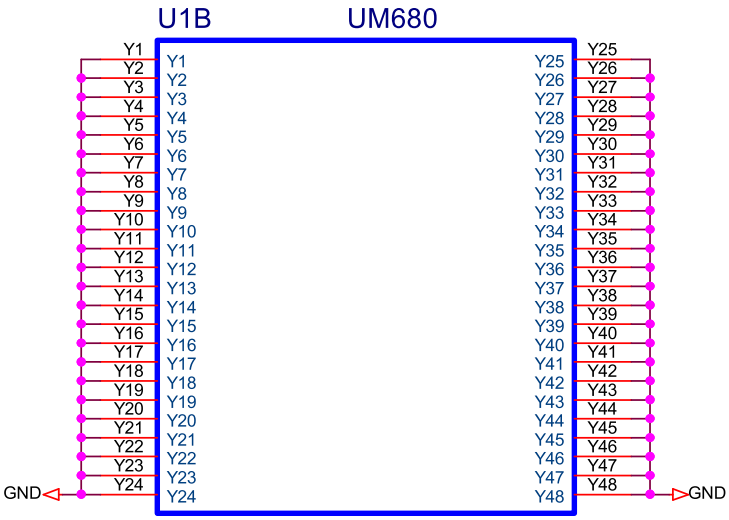


Figure 2-2 UM680 GND Pads

2.1 Main Power VCC

The working voltage range of the UM680 module is 2.7 V to 3.6 V.

Note:

- The VCC initial level when powered on needs to be less than 0.4 V.
- The VCC ramp when powered on needs to be monotonic, without plateaus.
- The voltages of undershoot and ringing need to be within 5% of VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μs to 10 ms.
- Power-on time interval: The time interval between the power-off (VCC < 0.4 V) to the next power-on needs to be larger than 500 ms.

2.2 Backup Power V_BCKP

When using hot start, please provide backup power for the UM680 module. The input range of V_BCKP is 2.0 V to 3.6 V.

Note:

- The V_BCKP initial level when powered on needs to be less than 0.4 V.
- The V_BCKP ramp when powered on needs to be monotonic, without plateaus.
- The voltages of undershoot and ringing need to be within 5% of V_BCKP.
- V_BCKP power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μs to 10 ms.
- Power-on time interval: The time interval between the power-off (V_BCKP < 0.4 V) to the next power-on needs to be larger than 500 ms.
- When the hot start is not used, connect V_BCKP to VCC or a standalone power source. Do not connect it to ground or leave it floating.

2.3 Active Antenna Power Supply

The antenna bias circuit consists of the anti-surge components, filter inductors, and ESD protection. The ESD protection diode should support high-frequency signals (above 2000 MHz).

- It is not recommended to use VCC_RF to supply power to the antenna, because it has not been optimized for anti-lightning strikes and anti-surges due to the compact size of the module.
- The antenna bias (ANT_BIAS) and the module's main power supply (VCC) should use separate power rails to reduce the risk of damage to the module. If ANT_BIAS and VCC use the same power rail, the ESD, surge and overvoltage generated at the antenna will be directly applied to VCC, which may cause damage to the module.

Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.

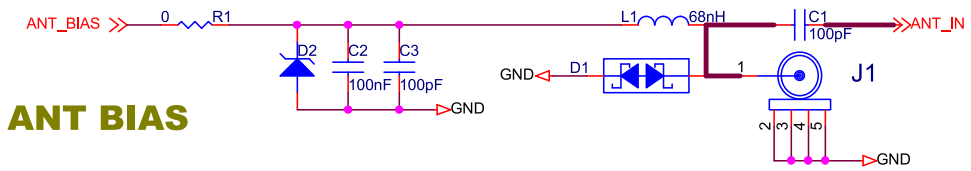
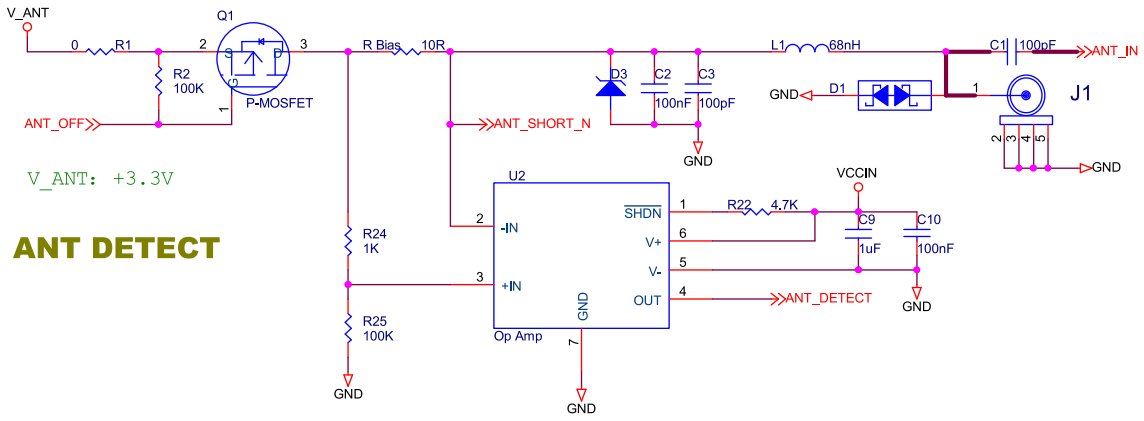


Figure 2-3 Antenna Bias Circuit

2.4 Antenna Detection Circuit

The antenna detection circuit is shown as follows:



Note: I/O Buffer is required when V_ANT&VCCIN voltage not matched

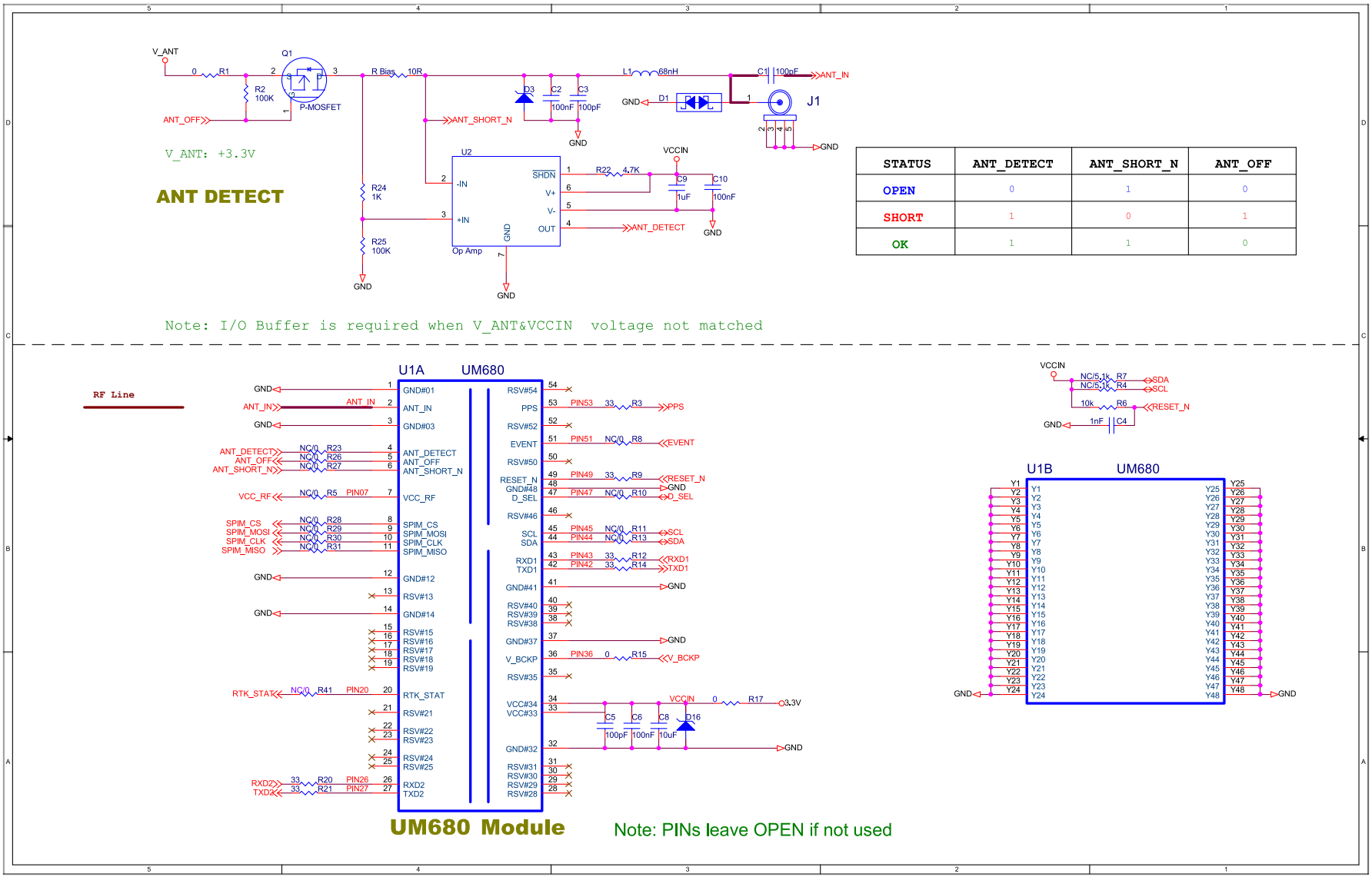
Figure 2-4 Antenna Detection Circuit

Status	ANT_DETECT	ANT_SHORT_N	ANT_OFF
Open	0	1	0
Short	1	0	1
OK	1	1	0

2.5 Reset Circuit

UM680 supports system reset. The RESET_N pin is active low and the active time is required to be no less than 5 ms.

3 Appendix: Schematics of Reference Design



STATUS	ANT_DETECT	ANT_SHORT_N	ANT_OFF
OPEN	0	1	0
SHORT	1	0	1
OK	1	1	0

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